MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2017/18

ECE2216 MICROCONTROLLER AND MICROPROCESSOR SYSTEMS

(All sections / Groups)

12 OCTOBER 2017
2:30 p.m. – 4:30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This Question paper consists of 10 pages including cover page and appendix with 4 Questions only.

2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) Two **signed** binary numbers are given as below:

$1110\ 0001_2$

$1100\ 0101_2$

i. Find the decimal equivalent value of these numbers. Show the computation steps. [3 marks]

ii. Add these two numbers in binary format. Identify the result as a positive or a negative number. Comment on the result obtained. [2 marks]

iii. Find the decimal equivalent of the result obtained in Q1(a)(ii). Show the computation steps. [2 marks]

iv. Convert the binary number obtained from Q1(a)(ii) to octal and hexadecimal number. [2 marks]

(b) There are many types of registers being used in Central Processing Unit (CPU). Describe the function of these registers: *Program Counter*, *Instruction Register* and *Address Register*. [6 marks]

(c) Highlight any **FIVE** features or specifications of **Intel 8051 microcontroller**. [5 marks]

(d) A memory structure of a microcontroller is shown in Figure Q1(d).

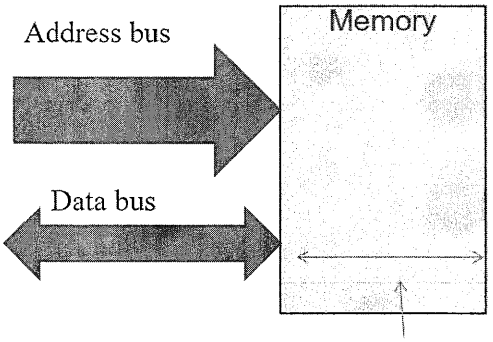


Figure Q1(d)

i. What is the size of the data bus? [1 mark]

ii. If the memory location is 14M, what is the size of the address bus for the memory structure shown in Figure Q1(d)? Show the computation steps. [3 marks]

iii. What is the maximum memory capacity that can be supported by the data bus and address bus obtained in Q1(d)(i) and Q1(d)(ii) above. [1 mark]

Continued ...

Question 2

(a) The active register bank in the 8051 microcontroller can be selected by modifying two bits in the PSW register. Briefly describe which two bits should be modified and the values to be used to select each register bank. Write an instruction to select Register Bank 2. [4 marks]

(b) What is address decoding? Design a memory system using 8K*8bits ROM and RAM ICs to form 24K*8bits of ROM and 24K*8bits of RAM. [11 marks]

(c) How a microcontroller can perform logical NAND operation using three inputs and one output NAND gate configuration. Justify your answer with flow chart. State the advantages and disadvantages in using a microcontroller compared to logic gates for the above operation. [8 marks]

(d) If an 8051 is operating from a 10 MHz crystal. What is the frequency of the waveform on ALE? Assume the software is not accessing external RAM. [2 marks]

Continued...

Question 3

(a) The machine codes of an instruction sequence for the 8051 microcontroller are shown in Table Q3(a).

Table Q3(a)

Address	Machine codes
0000H	86H 30H
0002H	79H 5AH
0004H	65H 31H

i. Convert the machine codes to the corresponding assembly instructions. [3 marks]

ii. Identify the addressing mode of the **source** and **destination** operands for the **THIRD** instruction. [2 marks]

iii. If a 12MHz crystal oscillator is used with the 8051 microcontroller, determine the total time for the microcontroller to execute this instruction sequence. [2 marks]

Hint: Refer to the opcode map in the Appendix.

(b) An assembly program for the 8051 microcontroller has been written by an embedded system developer.

```
      ORG 0000H
      MOV A, #0
      MOV R0, #30H
      MOV R1, #40H
      MOV R2, #4
      MOV R3, A
      MOV R4, A
LOOP: MOV A, @R0
      MOV B, A
      RLC A
      JNC SKIP
      MOV A, B
      ANL A, #7FH
      CPL A
      INC A
      INC R3
      SJMP NEXT
SKIP: MOV A, B
      INC R4
NEXT: MOV @R1, A
      INC R0
      INC R1
      DJNZ R2, LOOP
      SJMP $      ; program stops here
      END
```

Code Listing Q3(b)

Continued...

The contents of selected internal RAM from addresses 30H to 39H before the program is executed are shown in Table Q3(b).

Table Q3(b)

Address	30H	31H	32H	33H	34H	35H	36H	37H	38H	39H
Contents	97H	6EH	F1H	ACH	5EH	6FH	12H	23H	34H	45H

As an intern at the company, you are required to carry out the following tasks for the program listed in Code Listing Q3(b):

i. Analyze the program to determine the address of the affected memory locations in the internal RAM and their final contents after the program has been executed. [4 marks]

ii. Determine the final contents of registers R3 and R4 after the program has been executed. [2 marks]

iii. Calculate the address represented by the label "LOOP". [2 marks]

Hint: Refer to the opcode map in the Appendix.

(c) The MCS-51 instruction sequence in Code Listing Q3(c) has been written to carry out the following arithmetic operation: $A = (12_{10} + 5_{10}) \times (51_{10} - 39_{10})$

```
MOV A, #12
ADD A, @5
MOV B, A
MOV A, #51
SUBB A, #39
MUL BA
```

Code Listing Q3(c)

i. Analyse the instruction sequence to identify **TWO** wrong instructions and provide the corrected instructions. [3 marks]

ii. If the corrections have been done, determine the final contents of accumulator A after all six instructions have been executed. [2 marks]

(d) Write an assembly program for the 8051 microcontroller to generate a 10 kHz square wave (50% duty cycle) at pin P0.0 by using Timer 1 operating in Mode 2. Assume that the microcontroller is operating with a 12 MHz crystal oscillator. [5 marks]

Continued...

Question 4

(a) An 8051 microcontroller is equipped with an on-chip serial port for communication with external devices using UART.

i. Design an instruction sequence to initialize the on-chip serial port to Mode 1 with baud rate of 4800 (with SMOD = 1). Use Timer 1 and Mode 2 with an oscillator frequency of 11.0592 MHz [5 marks]

ii. Write a subroutine called "Ready" to transmit the string "Ready" serially via UART. [5 marks]

(b) As an intern in your company, you need to carry out the following task.

```
MOV IE, #8BH
MOV IP, #04H
```

Figure Q4(b)

i. Analyse the instruction sequence shown in Figure Q4(b) for an 8051 microcontroller. Determine the interrupts that have been enabled and the priority of each enabled interrupts. [3 marks]

ii. If the 8051 microcontroller is connected to a 12 MHz crystal oscillator, write an assembly program to generate a 200 Hz waveform with 50% duty cycle at pin 1.0 of the 8051 microcontroller using Timer 0 interrupt. Show all calculations involved. [8 marks]

(c) Sketch the circuit diagram to interface a keypad with 20 keys (arranged in 5 rows x 4 columns) to an 8051 microcontroller. Use P1 (LSB) for columns and P2 (LSB) for rows. [4 marks]

End of Paper

APPENDIX

Special Function Register Formats

Interrupt Enable (IE)

Bit Addr.	AFH	-	-	ACH	ABH	AAH	A9H	A8H
Name	**EA**	**-**	**-**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**

BIT	SYMBOL	FUNCTION (Enable=1, Disable=0)
IE.7	EA	Global enable/disable. EA = 1, each individual source is enabled/disabled by setting/clearing its enable bit. EA = 0, disable all interrupts.
IE.6	-	Undefined
IE.5	-	Not implemented in 8051. ET2 for 8052.
IE.4	ES	Serial port interrupt enable bit.
IE.3	ET1	Timer 1 interrupt enable bit.
IE.2	EX1	External interrupt enable bit.
IE.1	ET0	Timer 0 interrupt enable bit.
IE.0	EX0	External interrupt enable bit.

Interrupt Priority (IP)

Bit Addr.	-	-	-	BCH	BBH	BAH	B9H	B8H
Name	**-**	**-**	**-**	**PS**	**PT1**	**PX1**	**PT0**	**PX0**

BIT	SYMBOL	FUNCTION (Enable=1, Disable=0)
IP.7	-	Undefined
IP.6	-	Undefined
IP.5	-	Not implemented in 8051. PT2 for 8052.
IP.4	PS	Serial port interrupt priority bit.
IP.3	PT1	Timer 1 interrupt priority bit.
IP.2	PX1	External interrupt priority bit.
IP.1	PT0	Timer 0 interrupt priority bit.
IP.0	PX0	External interrupt priority bit.

Interrupt Vectors

Interrupt Source	Flag	Vector Address
System Reset	RST	0000H
External 0	IE0	0003H
Timer 0	TF0	000BH
External 1	IE1	0013H
Timer 1	TF1	001BH
Serial Port	RI & TI	0023H
Timer 2 (8052)	TF2 or EXF2	002BH

Program Status Word (PSW)

Bit Addr.	D7H	D6H	D5H	D4H	D3H	D2H	-	D0H
Name	**CY**	**AC**	**F0**	**RS1**	**RS0**	**0V**	**-**	**P**

Serial Control (SCON)

Bit Addr.	9FH	9EH	9DH	9CH	9BH	9AH	99H	98H
Name	**SM0**	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

BIT	**SYMBOL**	**FUNCTION**
SCON.7	SM0	Serial port mode bit 0 (see Table A.1).
SCON.6	SM1	Serial port mode bit 1 (see Table A.1).
SCON.5	SM2	Serial port mode bit 2; enables multiprocessor communications in modes 2 and 3; RI will not be activated if received 9th bit is 0. In mode 1, if SM2 = 1, then RI will be activated only if a valid stop bit was received. In mode 0, SM2 should be 0.
SCON.4	REN	Receiver enable; must be set to receive characters.
SCON.3	TB8	Transmit bit 8; 9th bit transmitted in modes 2 and 3; set/cleared by software.
SCON.2	RB8	Receive bit 8; 9th bit received.
SCON.1	TI	Transmit interrupt flag; set at end of character transmission; cleared by software.
SCON.0	RI	Receive interrupt flag; set at end of character reception; cleared by software.

Table A.1 The 8051 Serial Port Mode Selection

SM0	**SM1**	**Mode**	**Description**	**Baud Rate**
0	0	0	Shift register	Fixed
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fixed
1	1	3	9-bit UART	Variable

PCON (Power Control)

Bit	7	6	5	4	3	2	1	0
Name	**SMOD**	**-**	**-**	**-**	**GF1**	**GF0**	**PD**	**IDL**

BIT	**SYMBOL**	**FUNCTION**
7	SMOD	Double the serial port baud rate when it is set to 1
3	GF1	General purpose flag bit 1
2	GF0	General purpose flag bit 0
1	PD	Activate the microcontroller power-down mode when it is set to 1
0	IDL	Activate the microcontroller idle mode when it is set to 1

Timer Control (TCON)

Bit Addr.	8FH	8EH	8DH	8CH	8BH	8AH	89H	88H
Name	**TF1**	**TR1**	**TF0**	**TR0**	**IE1**	**IT1**	**IE0**	**IT0**

BIT	SYMBOL	FUNCTION
TCON.7	TF1	Timer-1 overflow flag. Set by hardware on overflow. Cleared by hardware when processor vectors to interrupt routine. Must be cleared by software when not involve interrupt
TCON.6	TR1	Timer-1 run control bit. Set/cleared by software to turn timer/counter on/off.
TCON.5	TF0	Timer-0 overflow flag. Do the same function as TF1 but for Timer-0.
TCON.4	TR0	Timer-0 run control bit. Do the same function as TR1 but for Timer-0.
TCON.3	IE1	External interrupt-1 edge flag. Set by hardware when interrupt-1 falling edge is detected. Cleared by hardware when interrupt is processed.
TCON.2	IT1	Interrupt-1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
TCON.1	IE0	External interrupt-1 edge flag. Do the same function as IE1 but for external interrupt-0.
TCON.0	IT0	Interrupt-0 Type control bit. Do the same function as IT1 but for external interrupt-0.

Timer Mode (TMOD)

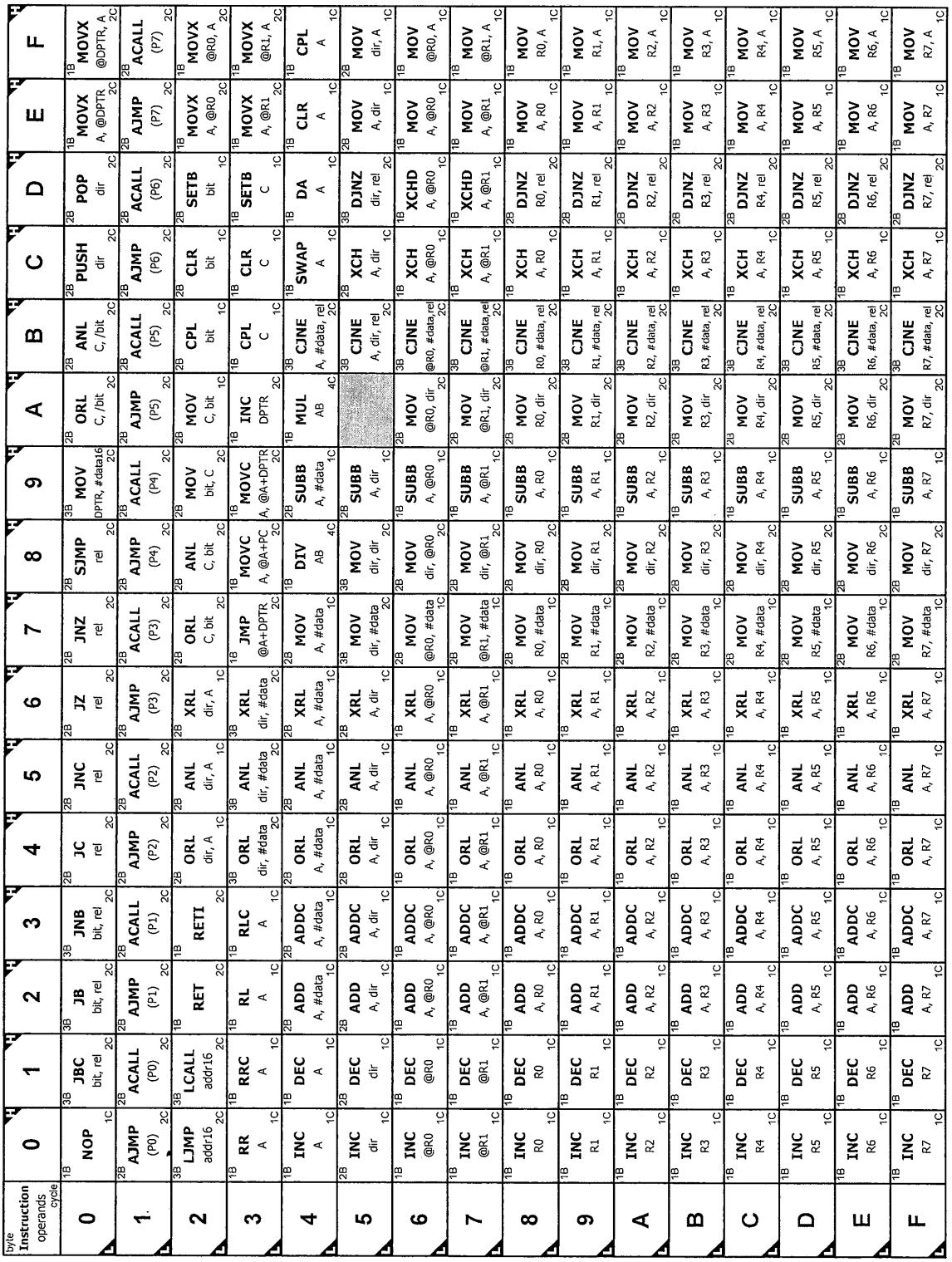
Bit	7	6	5	4	3	2	1	0
Name	**GATE**	**C/T**	**M1**	**M0**	**GATE**	**C/T**	**M1**	**M0**

BIT	SYMBOL	FUNCTION
TMOD.7	GATE1	When this bit is set the timer will only run when INT1 (P3.3) is high (hardware control). When this bit is cleared the timer will run regardless of the state of INT1 (software control).
TMOD.6	C/T1	Timer / Counter select bit. C / $\overline{T}$ = 0 → Timer operation. C / $\overline{T}$ = 1 → Counter operation.
TMOD.5	M1	Mode selection bits (see Table A.2). [for timer 1]
TMOD.4	M0	Mode selection bits (see Table A.2). [for timer 1]
TMOD.3	GATE0	Exactly the same function as GATE1 but for Timer0
TMOD.2	C/T0	Exactly the same function as C/T1 but for Timer0
TMOD.1	M1	Mode selection bits (see Table A.2). [for timer 0]
TMOD.0	M0	Mode selection bits (see Table A.2). [for timer 0]

Table A.2 Timer Mode Selection

M1	M0	Timer Mode	Description of Mode
0	0	0	13-bit Timer
0	1	1	16-bit Timer
1	0	2	8-bit auto-reload
1	1	3	Split timer mode

Opcode Map


byte
Instruction
operands
cycle
0 1 2 3 4 5 6 7 8 9 A B C D E F
0 NOP JBC JB JNB JC JNC JZ JNZ SJMP MOV ORL ANL PUSH POP MOVX MOVX
1 AJMP ACALL AJMP ACALL AJMP ACALL AJMP ACALL ACALL ACALL AJMP ACALL AJMP ACALL AJMP ACALL
2 LJMP LCALL RET RETI ORL ANL XRL ORL MOV ANL MOV CPL CLR SETB MOVX MOVX
3 RR RRC RL RLC ORL ANL XRL JMP MOVC DIV MOV INC CPL CLR SETB MOVX MOVX
4 INC DEC ADD ADDC ORL ANL XRL MOV SUBB MUL CJNE SWAP DA CLR CPL
5 INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH DJNZ MOV MOV
6 INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH XCHD MOV MOV
7 INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH XCHD MOV MOV
8 INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH DJNZ MOV MOV
9 INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH DJNZ MOV MOV
A INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH DJNZ MOV MOV
B INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH DJNZ MOV MOV
C INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH DJNZ MOV MOV
D INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH DJNZ MOV MOV
E INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH DJNZ MOV MOV
F INC DEC ADD ADDC ORL ANL XRL MOV SUBB MOV CJNE XCH DJNZ MOV MOV